REMARKS/ARGUMENTS

Claims 1-6, 15-26, and 31-34 along with newly added claims 35-38 are currently pending in the present patent application.

In an Office Action mailed December 5, 2006, the Examiner objected to Figures 1-5 for not including a suitable legend such as "Background Art" and objected to Figure 7 not including numbering for the top two layers in that figure. See Item 1 on pages 2 and 3 of the Office Action. The figures have been amended accordingly in replacement sheets that accompany this amendment.

The Examiner rejected claims 1-6 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,852,062 to Baker *et al.* ("Baker") in view of U.S. Patent No. 6,800,940 to Catabay *et al.* ("Catabay"). See Items 2 and 3 on pages 3-5 of the Office Action. The Examiner cites Figure 11 of Baker and asserts this figure shows the "floating gate region is insulated laterally, along a direction orthogonal to a plane including the floating gate, source, and drain regions, by a dielectric layer 60, 64 with a dielectric constant." *Id.* The Examiner cites Figure 4 of Catabay for disclosing the layer 30 having a low dielectric constant with a value between 1 and 3.9. *Id.*

Figure 11 of Baker is reproduced below.

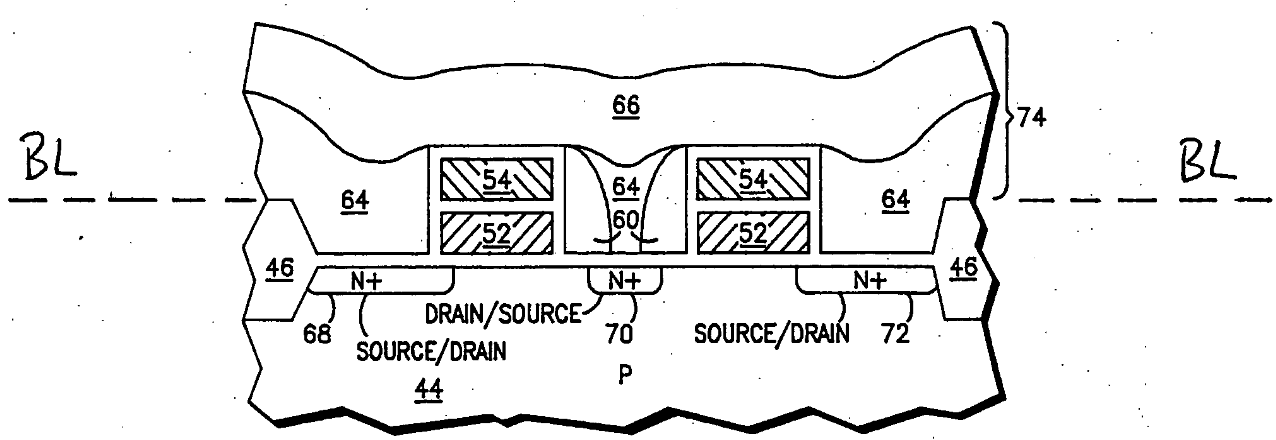

FIG. 11

A dotted line labeled X1-X1 has been added to Figure 11 to assist the present discussion of this figure. The plane of Figure 11 or the plane including the line BL-BL is a plane that is parallel to the bit lines of the memory structure disclosed in Baker. The bit

lines are associated with columns of memory cells in the memory-cell array structure of Baker, as is conventional in the art. Rows of memory cells in the array extend orthogonally to the columns of memory cells and thus in a direction extending into and out of plane of Figure 11. This is illustrated in Figure 17 of Baker, which is reproduced below.

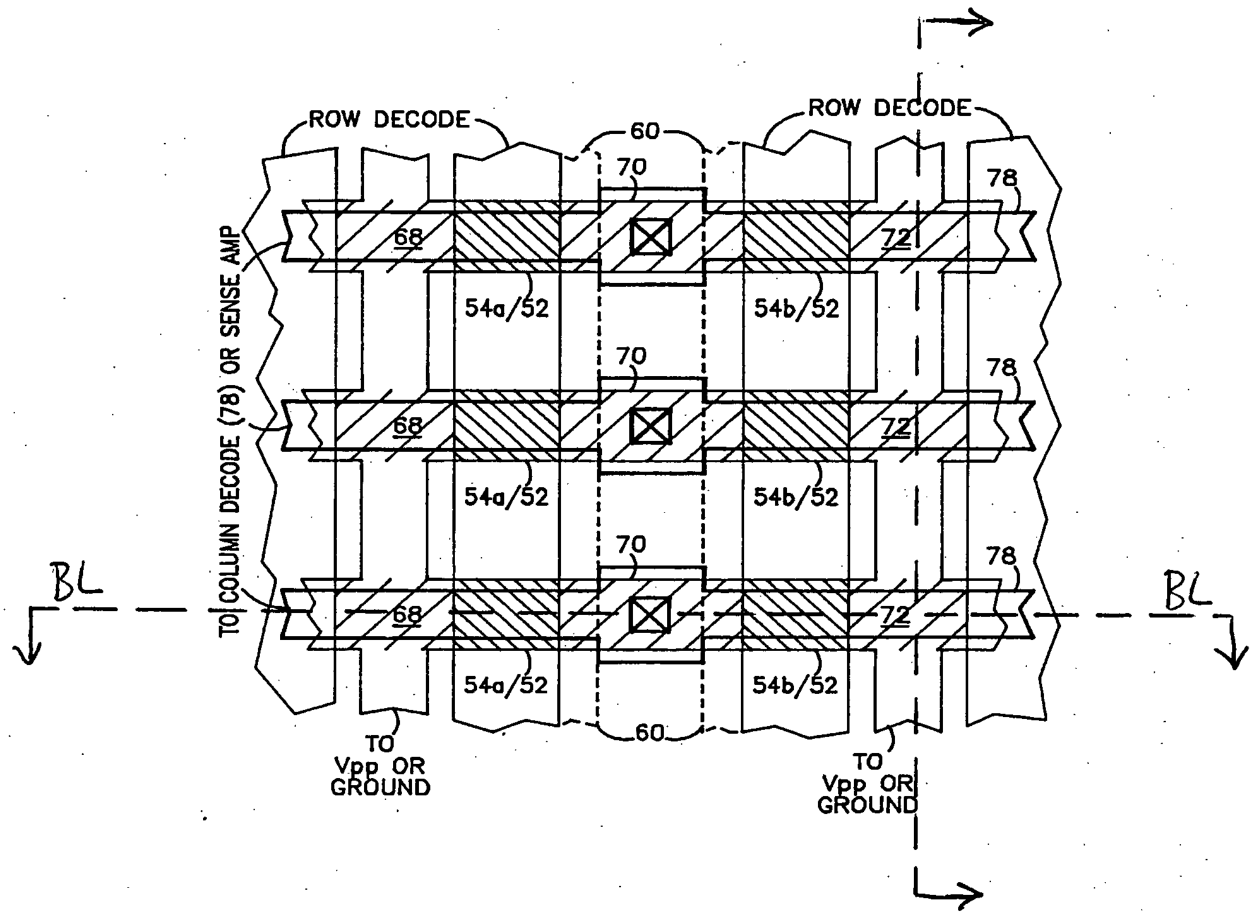

FIG. 17

In Figure 17, the line BL-BL extends horizontally across the page as shown since the bit lines likewise run horizontally across the page, as evidenced by the text on the left side of Figure 17 stating "TO COLUMN DECODE (78) OR SENSE AMP." The column or bit lines are connected to the column decode circuitry and/or sense amplifiers, as will be understood by those skilled in the art. The line BL-BL in Figure 17 shows the view along which the cross section of Figure 11 is taken. Since the bit lines are parallel to the line BL-BL and a plane containing that line, the word lines, being orthogonal to the bit lines, run vertically in Figure 17 as illustrated by the line WL-WL, which has been added to the figure

to aid the present discussion. The text "ROW DECODE" at the top of Figure 17 illustrates this fact since the word lines associated with rows of memory cells are connected to row decode circuitry, as will be understood by those skilled in the art.

Now referring to Figures 11 and 17, the source/drain 68, control gate 54 and floating gate 52 defining a transistor are in the plane of Figure 11. This plane contains line BL-BL and can be said to include the floating gate, source, and drain regions of the floating gate transistors. As discussed with reference to Figure 17, the word lines and associated rows of memory cells extend in a direction parallel to the line WL-WL that is orthogonal to the plane of Figure 11 (line BL-BL). The term "lateral" or "laterally" as used in the present application corresponds to the sides of the floating gates in a direction extending parallel to the line WL-WL or along a row of memory cells. Since the plane of Figure 11 includes the floating gate, source, and drain regions, the direction along the line WL-WL is along a direction orthogonal to a plane including the floating gate, source, and drain regions.

In this context, the inner spacers 60 and SOG layer 64 illustrated in Figure 11 do not insulate the two floating gates 52 laterally but instead insulate the floating gates in a direction parallel to the line BL-BL contained in the plane including the floating gate, source, and drain regions. The lateral sides of the floating gates correspond to the sides of the floating gates 52 that extend into and out of the page in the view of Figure 11, or along the line WL-WL in the view of Figure 17.

Claim 1 recites a non-volatile memory cell integrated on a semiconductor substrate including a floating gate transistor. The transistor includes a source region, a drain region, and a gate region projecting from the substrate and comprised between the source and drain regions. The gate region has a predetermined length and width and comprises a first floating gate region and a control gate region. The floating gate region is insulated laterally, along a direction orthogonal to a plane including the floating gate, source, and drain regions, by a dielectric layer with low dielectric constant value.

Baker neither discloses nor suggests a floating gate transistor having a floating gate region that is insulated laterally along a direction orthogonal to a plane including the floating gate, source, and drain regions by a dielectric layer with low dielectric constant value. The inner spacers 60 and layer 64 do not insulate the floating gates 52 laterally along the line WL-WL in the view of Figure 17. Instead, the inner spacers 60 and SOG

layer 64 illustrated in Figure 11 insulate the floating gates in a direction parallel to the line BL-BL contained in the plane including the floating gate, source, and drain regions.

With regard to Catabay, the Examiner points to layer 30 as being a low dielectric constant layer to reduce capacitive coupling between conduct lines. As explained above, even if such a low dielectric constant layer is used to replace the layers 60 and 64 the recited lateral insulation of the floating gate regions is not realized through the combination of Baker and Catabay. Furthermore, putting a low dielectric constant layer between conductive lines to reduce capacitive coupling has been well known for many years. To take this well known act and to then apply it to a new region on an integrated circuit is to oversimplify the problem. Regions on an integrated circuit are formed from selected materials for a variety of different reasons, such as desired electrical characteristics, ease of manufacture, affects of subsequent process steps on a region after formation of that region, and so on. The layer 30 is not positioned between the floating gates of transistors in a row of memory cells. Moreover, with the dimensions between floating gate regions in Baker and Catabay such a low constant dielectric was not needed since the spacing between adjacent floating gates was sufficient to prevent undue coupling even with the higher dielectric constant insulating material. As the distance between adjacent floating gate regions becomes sufficiently small (*i.e.*, on the order of less than 150-200nm) then such coupling becomes a factor, and it is this situation in which embodiments of the present invention help reduce this problem.

Independent claim 15 recites, in part, a memory cell matrix formed on a semiconductor substrate in which adjacent memory cells are coupled to the same word line of the memory cell matrix and are insulated from each other by a dielectric layer with low dielectric constant value. Independent claim 16 recites a memory-cell structure formed on a semiconductor substrate including a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate. Each memory cell in a respective row is coupled to a corresponding word line and each memory cell includes a floating gate region. The memory-cell structure includes an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of the memory cells in a row that are coupled to the same word line.

As discussed above with regard to claim 1, Baker does not disclose such a low dielectric material between adjacent floating gate regions of memory cells coupled to the

same word line (along the line WL-WL in Figure 17 above). The layers 60 and 64 are not along between the floating gate regions of memory cells coupled to the same word line but instead are between such regions of memory cells coupled to the same bit line (*i.e.,* along the direction BL-BL) and different word lines.

For these reasons, independent claims 15 and 16 are allowable and dependent claims 17-20 are allowable for at least the same reasons as claim 16 and due to the additional limitations added by each of these claims. Independent claims 21, 24, and 31 are allowable for similar reasons to those discussed with regard to claims 1, 15, and 16. All dependent claims not specifically discussed above are allowable for at least the same reasons as the associated independent claim and due to the additional limitations added by each of these claims.

New claims 35-38 recite that the low constant dielectric layer completely fills a space between adjacent memory cells coupled to the same word line and each is allowable for the same reasons as the associated independent claim and due to the additional limitations added by each of these dependent claims.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. **Should the Examiner consider any of the claims not allowable after consideration of this amendment, the undersigned request the Examiner contact him at (425) 455-5575 to discuss the outstanding through a telephone interview.** If any need for any fee in addition to that paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

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